

Notice of References Cited	Application/Control No. 09/819,773	Applicant(s)/Patent Under Reexamination GAUTHIER ET AL.	
	Examiner Russell Frejd	Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	BLAAUW et al., D. On-Chip Inductance Modeling, Proceedings of the 10th Great Lakes Symposium on VLSI, March 2000, pages 75-80.
	V	MICHALKA, T.L. Modeling the Power Rails in Leading Edge Microprocessor Packages, 48th IEEE Electronic Components and Technology Conference, May 1998, pages 598-604.
	W	BEKER et al., B. Tradeoffs in Modeling the Response of Power Delivery Systems of High-Performance Microprocessors, IEEE Conference on Electrical Performance of Electronic Packaging, October 2000, pages 77-80.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.